BL O/093/07

30 March 2007

PATENTS ACT 1977

APPLICANT Hewlett Packard Development Company L P

ISSUE Whether patent application number GB0317109.7 relates to a patentable invention

HEARING OFFICER P R Slater

DECISION

Introduction

1 Patent application GB0317109.7 entitled a "Method and apparatus for simplifying a circuit model" was filed on 22 July 2003 in the name of Hewlett Packard Development Company L P.The application claims priority from an earlier United States application US 10/213,960 filed on 7 August 2002. The application was published as GB2391660 on 11 February 2004.

2 Since the first examination report was issued on 13 May 2005, there have been a number of additional rounds of correspondence throughout which the examiner has maintained an objection that the invention was excluded from patentability under section 1(2) of the Act as being a program for a computer, a method for performing a mental act and/or mathematical method.

3 Having been unable to resolve the issue, the matter came before me to decide at a hearing on 6 October 2006 at which the applicant was represented by Mr John Brunner of Carpmaels & Ransford, assisted by Dr Gary Small.

4 Mr Brunner's argument at the hearing was based on the law as it then stood following the judgment laid down in *CFPH LLC's Application*[1]. However on 27 October 2006, shortly after the hearing, the Court of Appeal handed down its judgment in the matters of *Aerotel Ltd v Telco Holdings Ltd* and *Macrossan's Application*[2] (*Aerotel/Macrossan*) which approved a new test for assessing patentability under Section 1(2). The examiner therefore issued a further letter on the 12 January 2007, re-assessing the application in light of this new test, maintaining his earlier objection that the invention was excluded from

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[1] [2005] EWHC 1589 (Pat); [2006] RPC 5

[2] 2006] EWCA Civ 1371

patentability under Section 1(2) and giving the applicant an opportunity to make further submissions. Mr Brunner replied in a letter dated 30 January 2007.

The Application

5 The application relates to the computer simulation of integrated circuits and in particular the creation of circuit models on which to run timing software. It is well known that for accurate simulation and testing, timing software requires circuit models which incorporate the effects of parasitic resistance and capacitance resulting, for example, from on chip-wiring or interconnects. However, the more complex the model, the more time and memory are required to run the software. It is often therefore desirable to simplify the model by eliminating elements of resistance and capacitance, so that the timing software will run in reasonable time and memory. This has been achieved in the past by removing all resistances and capacitances having values below a certain threshold. However, this tends to result in an oversimplification of the model, reducing its accuracy and introducing significant errors into the timing analysis.

6 In essence, the invention provides a new way of simplifying circuit models in which the various inputs to the so called “active elements” e.g. transistors are examined to see if they can be simplified by removing elements of resistance. Typically, each input comprises a branch resistance, and one or more input and/or parasitic capacitances. The time constant at each input is calculated and compared to a threshold value. If the time constant is below the threshold, then the resistance present at the input is removed from the circuit and the remaining capacitances where possible are combined. The process is then repeated in an iterative manner until no further simplification of the model is possible.

7 There are currently three sets of claims for me to consider. The preferred set of claims (“the Main Request”) is equivalent to those originally filed on 22 July 2003 and includes 3 independent claims which read as follows:

1. Apparatus 300 for simplifying a circuit model 304 comprising digital computing apparatus having memory 302, the memory 302 having recorded therein machine-readable instructions 306 for performing steps comprising: identifying 201 an active device model 104 of a circuit model, the circuit model comprising a plurality of interconnected active device models 104, resistance models 110, and capacitance models I I8, the identified device model 104 having an input coupled to a first circuit node 105 coupled to a resistance model 110, where the resistance model is coupled to a second circuit node 107 of the circuit model; calculating an input capacitance of the active device model 104; computing 206 a time constant of the first circuit node 105 from a resistance of the resistance model 110 and a total capacitance of the first circuit 15 node 105, where the total capacitance of the first circuit node includes the input capacitance of the active device; comparing 208 the time constant to a threshold, and, if the time constant is less than the threshold, modifying the circuit model 100 to remove the resistance model and couple the input of the active device model 104 to the second circuit node 107; and

repeating 218 the steps of identifying, calculating, computing, and comparing; for a plurality of active devices of the circuit model.

5. A computer program product comprising a machine readable media having recorded thereon machine readable instructions comprising instructions for execution of the steps identifying 201 an active device model 104 of a circuit model 100, the circuit model comprising a plurality of interconnected active device models 104, resistance models 110, and capacitance models I I8, the identified device model 104 having an input coupled to a first circuit node 105 coupled to a resistance model 110, where the resistance model is coupled to a second circuit node 107 of the circuit model; calculating an input capacitance of the active device model 104; computing 206 a time constant of the first circuit node 105 from a resistance of the resistance model 110 and a total capacitance of the first circuit node 105, where the total capacitance of the first circuit node includes the input capacitance of the active device; comparing 208 the time constant to a threshold, and, if the time constant is less than the threshold, modifying the circuit model 100 to remove the resistance model couple the input of the active device model 104 to the second circuit node 107; and repeating 218 the steps of identifying, calculating, computing, and comparing for a plurality of active devices of the circuit model.

8. A method of simplifying a circuit model, the circuit model comprising a plurality of interconnected active device models, resistance models, and capacitance models, the method comprising the steps of: identifying an active device having an input coupled to a first circuit node coupled to a resistance, where the resistance model is coupled to a second circuit node of the circuit model; calculating an input capacitance of the active device; computing a time constant of the resistance and a total capacitance of the first circuit node, where the total capacitance of the first circuit node includes the input capacitance of the active device; comparing the time constant to a threshold; and if the time constant is less than the threshold, removing the resistance from the circuit model and coupling the input of the active device to the second circuit node.

Auxilliary requests

8 Mr Brunner filed two alternative sets of claims for me to consider ("Auxiliary Requests 1 & 2"). Auxiliary Request 1 was filed on 3 October 2006 prior to the hearing and again includes three independent claims wherein original claims 1 and 8 of the Main Request have been amended so as to relate to an apparatus and a method for *analysing* a circuit model. Furthermore, independent claims 1, 5 and 8 have been amended to include the additional step of *performing a timing analysis of the circuit model as a whole*. Auxiliary Request 2, which was filed on 30 January 2007, contains only two independent claims 1 and 5 which are again based on original claims 1 and 8 of the Main Request but include the additional feature of *merging any capacitance models coupling both the first circuit node 105 and second circuit node 107 to a common node and retaining any capacitance model coupling the first node 107 to a node which is not coupled with a capacitance model to the circuit node 107*. Furthermore, original claims 5 to 7 and 16, which related to a computer program product, have been deleted.

The Law and its interpretation

9 The examiner has reported that the application is excluded from patentability under section 1(2) of the Act, as relating to a program for a computer, a method for performing a mental act. The relevant parts of section 1(2) read:

> *1(2) It is hereby declared that the following (among other things) are not inventions for the purposes of this Act, that is to say, anything which consists of:*
>
> *(a) a discovery, scientific theory or* mathematical method*;*
>
> *(b) a literary, dramatic, musical or artistic work or any other aesthetic creation whatsoever;*
>
> *(c) a scheme, rule or method for performing a mental act, playing a game or doing business, or a program for a computer;*
>
> *(d) the presentation of information;*

10 As regards the interpretation of section 1(2), my approach will be governed by the judgment of the Court of Appeal in *Aerotel/Macrossan* and the Practice Notice issued by the Patent Office on 2 November 2006. In Aerotel/Macrossan the court reviewed the case law on the interpretation of section 1(2) and approved a new four-step test for the assessment of patentability, namely:

1) Properly construe the claim
2) Identify the actual contribution
3) Ask whether it falls solely within the excluded matter
4) Check whether the actual contribution is technical in nature.

11 However, the fourth step of checking whether the contribution is technical in nature may not be necessary because the third step – asking whether the contribution is solely of excluded matter – should have covered that point (see paragraphs 45 – 47 of the judgment).

12 Finally, I note that by virtue of section 130(7) of the Act section 1(2) is so framed as to have, as nearly as practicable, the same effects as the corresponding provisions of the European Patent Convention. However, the reliance that I can place on decisions of the Boards of Appeal of the European Patent Office under the corresponding Article 52 of the EPC must now be limited in view of the contradictions in these noted by the Court of Appeal in *Aerotel/Macrossan* and its express refusal to follow EPO practice.

Arguments and analysis

13 Having regard to the first step of the *Aerotel/Macrossan* test, the construction of the claims has not been disputed.

14 The second step requires me to identify the contribution; paragraph 43 of the judgement suggests that I need to identify what the inventor has added as a matter of substance to human knowledge. The examiner, in his letter dated 12 January 2007, considered the contribution to lie *in "a method, apparatus for simplifying a circuit model by removing parasitic capacitance and resistance based on time constant values".* Mr Brunner argues that the contribution lies in the specific way in which the circuit model is simplified, that is, the invention provides a *"new way of simplifying a circuit model"*. Indeed, as Mr Brunner points out, the invention as claimed does not require the removal of parasitic capacitance merely resistance. In support of his arguments, he refers to the discussion of the prior-art in the specification and in particular the disclosure in *Sheehan*[3]. It is clear from the specification that techniques are already well known for simplifying complex circuits in this type of context. One of the simplest solutions is merely to remove all resistances and capacitances having values below a certain threshold as described in paragraph [0008]. However, this can introduce significant errors into the simulation. *Sheehan* describes an alternative way of simplifying a circuit model by evaluating RC time constants at specific nodes in the model, classifying them as either quick, normal or slow nodes, and then eliminating the quick and slow nodes from the model. Having carefully considered the prior art, I am satisfied that the contribution is as Mr Brunner suggests, a new method of simplifying a circuit model.

15 The third step requires me to consider whether the contribution lies solely in excluded matter. I will begin by considering the method as defined in claims 8 to16 of the Main Request, in which a series of calculations are performed in order to simplify a circuit model. I feel that this lies at the very heart of the invention and best reflects the actual contribution. The examiner considers these claims to constitute a mental act. Mr Brunner accepts that an operator could, when presented with a circuit model in the form of a circuit diagram or representation on paper or screen, perform the method as claimed, modifying the circuit diagram as a result. However, he argues that this is not the case, here the model is not merely a representation of the circuit but a computer equivalent of the physical circuit implemented in program code, which has the functionality of the actual circuit, and it is this functionality which is modified as a result of performing the method. Hence the contribution is more than a mental act, as it involves not only modifying the model but also the functionality of the model and the underlying computer code. Furthermore, Mr Brunner would have me believe that you could implement the invention in hardware, with physical circuit elements representing the parasitic components, run the timing analysis in hardware and actually modify the physical circuit and that this in itself would not constitute a mental act. However, I am not convinced by Mr Brunner's arguments. Obviously, the method is intended for use on a computer, but as a matter of fact the claims are not so limited. The fact that you could in principle, implement the invention in hardware is misleading as this would detract from the whole purpose of the invention which is all about

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[3] "TICER: Realizable Reduction of Extracted RC Circuits, 1999 IEEE/ACM

running the model on a computer to speed up the timing software analysis. Indeed, it is my view that the method as defined is no more than a series of mental operations which could in principle be performed by a person using pen and paper, and as such the invention is excluded as a scheme, rule or method for performing a mental act.

16 I will now move on to consider the apparatus as defined in claims 1 to 4. Here, the examiner considers the contribution to be no more than a program for a computer. At the hearing, Mr Brunner argued that whilst the specific embodiment involves a computer model of the circuit it could equally well be implemented in hardware and as such the invention is not solely limited to a computer program. He again emphasised the fact that the invention did not merely result in a modified representation of the circuit model but that the actual underlying functionality of the circuit was being manipulated.

17 Furthermore, Mr Brunner in his letter of 30 January 2007 argues as follows:

> "…the invention of the present application is more than the execution of a known method using conventional computer program steps. The method of circuit model simplification embodied in the present invention is not known from the prior art. Therefore whether or not the invention is carried out by a suitably programmed computer should not detract from the fact that the actual contribution lies outside excluded subject matter. It is appreciated that a "circuit model" may be a sequence of instructions for example in the form of a "netlist", which is stored in computer memory (see paragraph [0023]) and that a computer program executing on the computer can manipulate the circuit model. This is entirely reasonable; almost all modern circuit designers use a computer to model circuit designs. Indeed, the circuit model is, to all intents and purposes, the physical circuit because a significant proportion of modern electronic circuits are implemented as a sequence of instructions in embedded integrated circuitry. The use of conventional circuit components to represent these instructions is useful because it allows a circuit designer to understand easily how the circuit might operate. In the context of the present invention, simplification of the circuit model is useful so that analysis of the circuit model can run in more reasonable time and memory. However, it will be appreciated that any simplification to the circuit model will have an effect on the functionality of the circuit model in just the same way that modification of a physical circuit would have the same effect.
>
> In essence, the circuit model is a simplification of the underlying program code and hardware which performs the equivalent function of a physical circuit represented by the circuit model. Thus when the apparatus and method of the invention simplifies the circuit model, it is modifying not only the model, but also the functionality of any circuit represented by the model. Thus, the "circuit model" can be seen as an easy-to-understand language for the underlying functionality performed by the equivalent object code which itself represents the underlying functionality performed by equivalent machine code. Modification of the source code will affect the structure and functionality of both the object code and machine code. In essence, source code, object code and machine code are data stored in memory. It is established practice of your office that new methods of operating on source code, object code and machine code (e.g. in compilers) should not be excluded from patentability. As explained above, the contribution of the present invention is a new way of simplifying a circuit model. Clearly, this contribution is not limited solely to categories which are excluded under section 1(2) of the Act"

18 Again, I am not entirely convinced by Mr Brunner's arguments. It is clear in my mind that the apparatus as defined in claims 1 to 4 is nothing more than a conventional computer programmed to perform a series of instructions which enable the computer to simplify an existing model of a circuit. Indeed, the circuit model itself is implemented in program code, is manipulated by a program which modifies that code to generate a new model. The contribution lies in the specific instructions used to simplify the model and there is nothing to suggest that these instructions are anything other than standard computer instructions adapted for that purpose. This clearly points to the contribution being solely within the meaning of a computer program as set out in section 1(2).

19 Finally, it remains for me to consider the invention as defined in claims 5 to 7 which relate to a computer program product. Whilst the judgment in *Aerotel/Macrossan* maintains the emphasis on substance over form, it also characterises the first step as deciding what the monopoly is. On that basis it seems to me that in claims 5 to 7 the monopoly does not go beyond a program and as a consequence the contribution fails at step (3) under section 1(2)(c) as a program for a computer;

20 Having decided that the contribution relates solely to excluded matter, it is not necessary for me to proceed to the fourth step of considering whether or not the contribution is technical in nature.

Auxiliary requests

21 I do not consider the amended claims filed on 3 October 2006 and 30 January 2007 to have any material affect on the substance of the invention or indeed its contribution and hence also regard them as excluded under section 1(2) for the reasons I have outlined above.

Conclusion

22 I have found that the invention relates to a mental act and a program for a computer as such and is therefore not patentable. I have read the specification in its entirety and cannot identify anything that could form the basis of a patentable invention. I therefore refuse the application under section 18 as failing to meet the patentability requirements of section 1.

Appeal

23 Under the Practice Direction to Part 52 of the Civil Procedure Rules, any appeal must be lodged within 28 days.

P R SLATER
Deputy Director acting for the Comptroller